a first processor;
a second processor;
a first memory; and
a second memory;

said first processor having write access at any time to any location in said first memory and read access at any time to any location in said first memory and said second memory; and

said second processor having write access at any time to any location in said second memory and read access at any time to any location in said first memory and said second memory.

24. The apparatus recited in claim 23, wherein said first and second processors operate independently of each other.

25. The apparatus recited in claim 24, wherein said first and said second processors comprise processors dedicated to control separate and independent functions in a system.

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~~26.~~ The apparatus recited in claim ~~23~~, wherein at least one of said first and second processors is a streamlined signal processor.

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~~27.~~ The apparatus recited in claim ~~23~~, wherein at least one of said first and second processors is configured to control a servo loop function of a system.

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~~28.~~ The apparatus recited in claim ~~23~~, further comprising input circuitry configured to receive signals related to a function of a system to be controlled and

output circuitry configured to provide signals related to a function of said system to be controlled.

~~29.~~ The apparatus recited in claim ~~23~~, wherein at least one of said first and second processors is configured to execute a statically scheduled control routine.

~~30.~~ The apparatus recited in claim ~~23~~, wherein said first memory and said second memory comprise respective portions of a same memory.

31. An apparatus comprising a plurality of processors and a plurality of memories, each processor having write access at any time to only a particular one of said memories and read access at any time to any of said memories.

32. The apparatus recited in claim 31, wherein said first memory and said second memory comprise respective portions of a same memory.

33. The apparatus recited in claim 31, wherein at least one of said processors in said plurality operates independently of other processors in said plurality.

~~34.~~ The apparatus recited in claim ~~31~~, wherein at least one of said processors controls a servo loop function of a system.